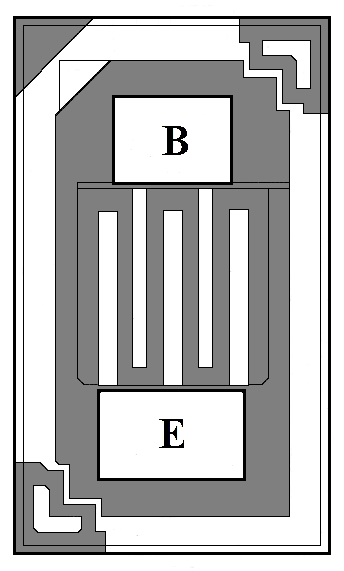
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.012”**

**.019”**



**.0032 x .0048**

**.0032 x .0038**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .0032” X .0048” B = .0032” X .0038”**

**Backside Potential:**

**Mask Ref: SMN**

**APPROVED BY: DK DIE SIZE .012” X .019” DATE: 7/19/23**

**MFG: ALLEGRO / SPRAGUE THICKNESS .006” P/N: 2N3250**

**DG 10.1.2**

#### Rev B, 7/19/02